

GENERAL DESCRIPTION

The VM3000 is a high performance, low noise digital MEMS microphone. It features a PDM output enabling multiplexing of two microphones on a single data line. The digital output has high immunity to RFI and EMI providing designers with more flexibility in the position of the mics and the routing of their wires in system. The VM3000 has an industry standard 3.5x2.65x1.3mm package.

The microphone is solder reflow compatible with no sensitivity degradation. It operates in environmentally harsh surroundings being dust and moisture resistant.

FEATURES

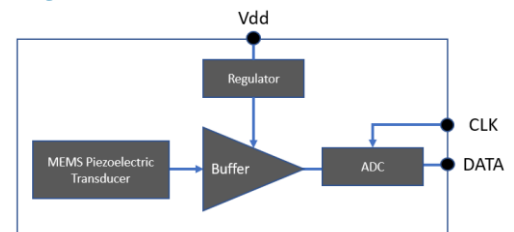
- Digital Output, Pulse Density Modulation (PDM)
- Less than 1 μ A current consumption in Sleep mode
- Ultra-fast startup, 200 μ Sec, from all modes
- Dust and moisture resistant, IP58
- Flat Frequency Response
- Sensitivity Matching
- Supports Dual Multiplexed Channels on DATA line
- RFI and EMI robust
- Industry standard 3.5 x 2.65mm LGA package footprint

APPLICATIONS

- Beamforming Arrays
- Smart Home Devices
- Outdoor Applications
- Wearables
- IP Security Cameras



BLOCK DIAGRAM



ORDERING INFORMATION

Product	Package Description	Quantity
VM3000AA	13" Tape and Reel	5,000

TYPICAL APPLICATION CIRCUIT

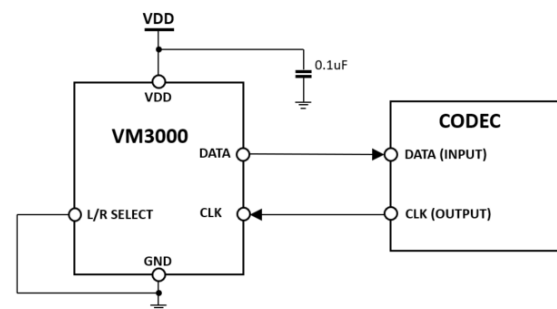


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SPECIFICATIONS

Table below shows **General Acoustic and Electrical specifications** at 25°C, VDD = 1.8 V, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	VDD		1.6	1.8	3.6	V
Sensitivity	SENS	1 kHz, 94 dB SPL	-27	-26	-25	dBFS
Output DC Offset				0		% FS
Roll Off Frequency		-3dB at 1KHz		100		Hz
Directivity			Omni			
Polarity		Increase in sound pressure	Increase in density of 1's			
Supply Current- Sleep Mode		VDD On, CLK Off (CLK must be logic LOW)		0.35		μA
Supply Current- Standby Mode		VDD On, CLK < 250 kHz No PDM Output		145		μA
Time to First Data Bit		Time from valid Vdd and CLK until first valid bit is driven on the DATA line. Output is Hi-Z until then.		0.1		mS
Startup Time		(Powered Down, Sleep, or Standby) → Active (Low Power or Normal Mode) Within ±0.5dB of actual sensitivity		0.2		mS
Mode-Change Time		Between any modes (Sleep, Standby, Low Power, Normal)		0.2		mS

Table below shows specifications for **Normal Mode** (1.1MHz < CLK < 4MHz) at 25°C, VDD = 1.8 V, CLK = 2.4MHz, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Signal-to-Noise Ratio	SNR	94 dB SPL at 1 kHz signal, 20Hz-20kHz, A-weighted Noise		62.5		dB(A)
Signal-to-Noise Ratio, Voice Band	SNR	94 dB SPL at 1 kHz signal, 20Hz-8kHz, A-weighted Noise		64		dB(A)
Total Harmonic Distortion	THD	94 dB SPL		0.1		%
		120dB SPL		1		
Acoustic Overload Point	AOP	10.0% THD		122		dB SPL
Power Supply Rejection Ratio	PSRR	VDD = 1.8, 1kHz, 100mV _{PP} Sine Wave		-76		dBFS/dBV
Power Supply Rejection	PSR	VDD = 1.8, 217Hz, 100mV _{PP} square wave, 20 Hz – 20kHz, A-weighted		-87		dB(A)
Supply Current		CLK = 1.536MHz		575		μA
		CLK = 2.4MHz		700		μA
		CLK = 3.072MHz		800		μA

Table below shows specifications for **Low Power Mode** (350kHz < CLK < 900kHz) at 25°C, VDD = 1.8 V, CLK = 768kHz, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Signal-to-Noise Ratio, Voice Band	SNR	94 dB SPL at 1 kHz signal, 20Hz-8kHz, A-weighted Noise		63		dB(A)
Total Harmonic Distortion	THD	94 dB SPL		0.1		%
		120dB SPL		1		
Acoustic Overload Point	AOP	10.0% THD		122		dB SPL
Power Supply Rejection Ratio	PSRR	VDD = 1.8, 1kHz, 100mV _{PP} Sine Wave		-76		dBFS/dBV
Power Supply Rejection	PSR	VDD = 1.8, 217Hz, 100mV _{PP} square wave, 20 Hz – 8kHz, A-weighted		-87		dB(A)
Supply Current		CLK = 768kHz		400		µA

DEVICE MODES

MODE	Conditions	Output on DATA Pin	Mode Transition Time to Low or Normal Power	Supply Current (Typical, µA)
OFF	VDD OFF	NA	200 µSec	NA
SLEEP	VDD ON, CLK OFF (LOGIC LOW)	NA	200 µSec	<1 µA
STANDBY	VDD ON, CLK ON (< 250 kHz)	NA	200 µSec	145 µA
LOW POWER	VDD ON, 350 kHz < CLK ON < 900 kHz	PDM	200 µSec	400 µA
NORMAL POWER	VDD ON, CLK ON > 1.1 MHz	PDM	NA	700 µA

CHANNEL SELECTION

Channel	Select	Asserts DATA on	Latch DATA on
Left	GND	Falling Edge of CLK	Rising Edge of CLK
Right	VDD	Rising Edge of CLK	Falling Edge of CLK

PDM DIGITAL SPECIFICATIONS

Parameter	Conditions	Min.	Typ.	Max.	Units
Logic Input High		0.65*VDD		VDD	V
Logic Input Low		-0.3		0.35*VDD	V
Logic Output High	I _{Load} = 0.5mA	0.7*VDD	VDD		V
Logic Output Low	I _{Load} = 0.5mA		0	0.3*VDD	AV
Driving Capability				100	pF

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Supply Voltage	-0.3 to +3.6	V
Sound Pressure Level	160	dB re 20 µPa
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-55 to +150	°C

ENVIRONMENTAL ROBUSTNESS

IP adherence is evaluated by 1kHz Sensitivity spec post stress

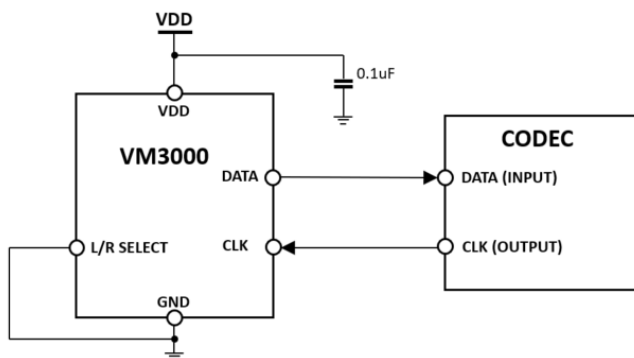
Ingress Protection Type	Description
Dust Resistance	IP5X;
Water Immersion	IPX8; 2 hours drying time, dry environment

RELIABILITY SPECIFICATIONS

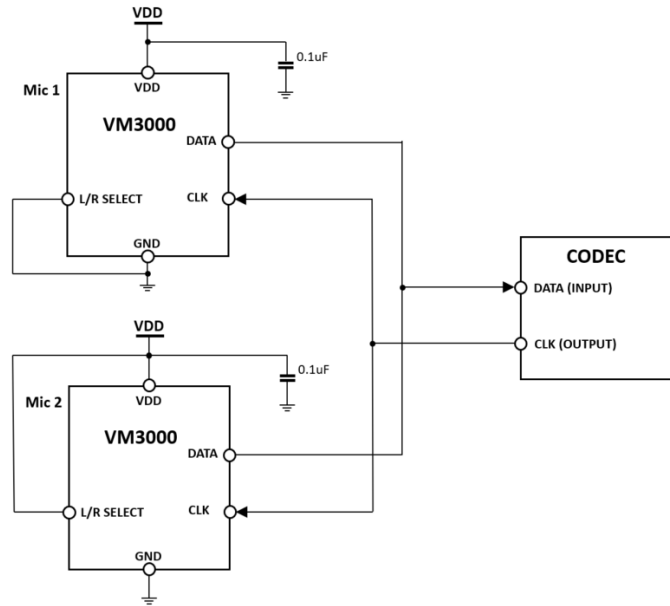
Stress Test	Description
Temperature Cycling Test	-40°C to +125°C, 850 cycles
High Temperature Operating Life	+125°C, 1000 hours, biased
High Temperature Storage	+125°C, 1000 hours, unbiased
Temperature Humidity Bias	+85°C, 85% RH, 1000 hours, biased
Reflow	3 reflow cycles with peak temperature of +260°C
ESD-HBM	3 discharge, all pins, ± 4kV
ESD-CDM	3 discharges, all pins, ± 750V

MICROPHONE OPERATION

The VM3000 is a Pulse Density Modulated (PDM) digital output microphone. It takes the audio signal from the Piezo MEMS element, amplifies it and samples at a very high rate, converting it to a single-bit stream PDM using a fourth order sigma delta modulator. This PDM data (DATA) is ready to be interfaced directly to a codec, applications processor or other compatible hardware. The master system (codec etc.) provides the master clock, CLK which defines the rate at which the bits are transmitted on the DATA line. The data is set on the rising or falling edge of the CLK, defined by the L/R Select pin, with L/R Select=GND (left) setting data on the falling edge, and L/R Select=Vdd (right) setting data on the rising edge. This allows two microphones to be connected to form a stereo configuration over a single DATA line. The CODEC or processor can then separate the bitstreams based on their alignment with the CLK edges.



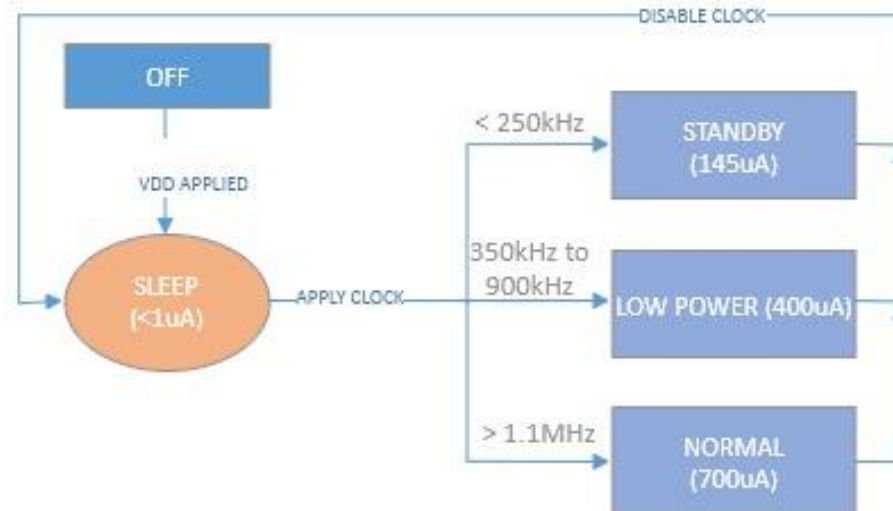
Typical Application Circuit for Mono Microphone Configuration (Left Channel Selected)



Typical Application Circuit for Stereo Microphone Configuration

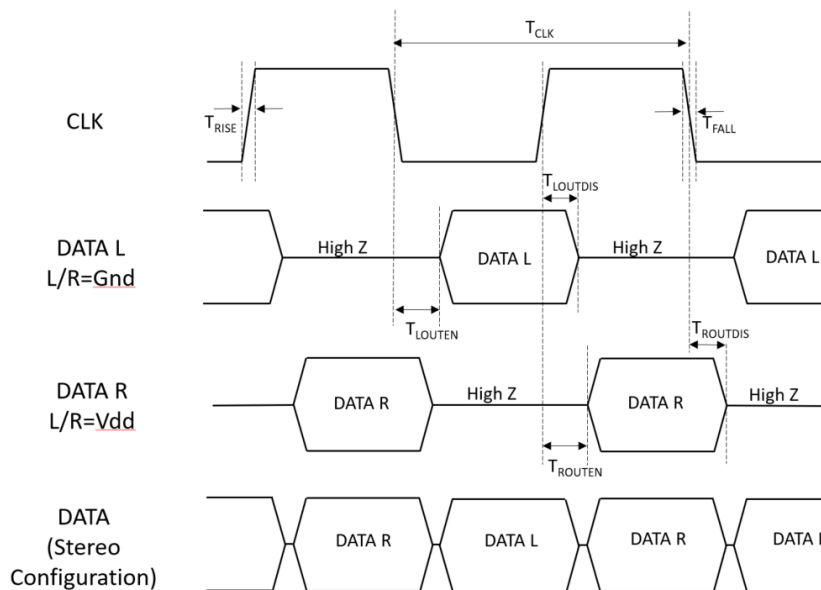
MICROPHONE MODES

The state diagram below shows the different modes and the associated current consumption.



VM3000 State Diagram

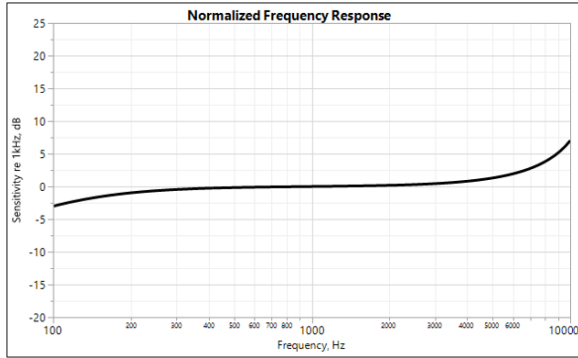
TIMING SPECIFICATIONS



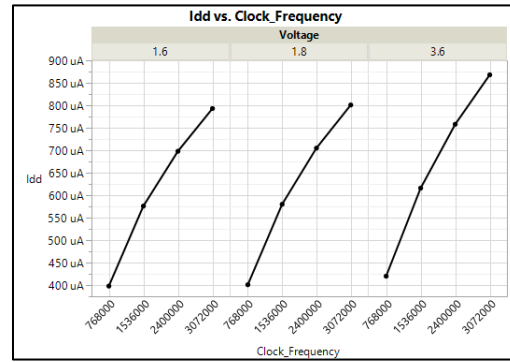
Timing Diagram for CLK, DATA L, DATA R in Stereo Configuration

Parameter	Conditions	Min.	Typ.	Max.	Units
T _{CLK}	CLK period	303		3636	nS
T _{RISE}	CLK Rise Time (10%-90% level)			25	nS
T _{FALL}	CLK Fall Time (90%-10% level)			25	nS
T _{LOUTEN}	DATA L driven after falling CLK edge	31	48	80	nS
T _{LOUTDIS}	DATA L disabled after rising CLK edge	9	17	30	nS
T _{ROUTEN}	DATA R driven after rising CLK edge	31	48	80	nS
T _{ROUTDIS}	DATA R disabled after falling CLK edge	9	17	30	nS

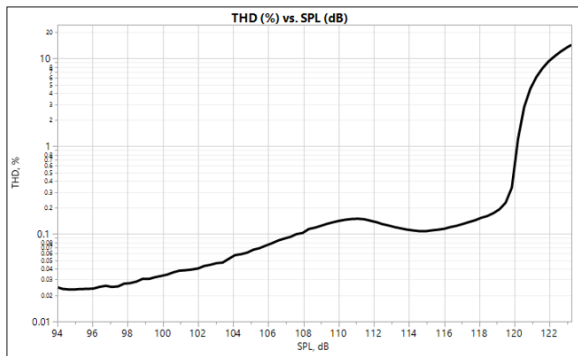
TYPICAL PERFORMANCE CHARACTERISTICS



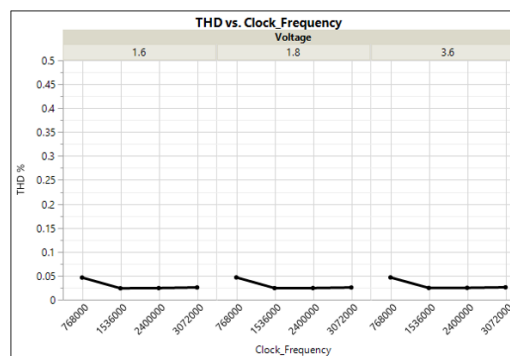
a. Normalized Frequency Response



c. Idd vs Clock over Vdd



b. THD (%) vs dB SPL



d. THD vs Clock Rate over Vdd

SOLDER REFLOW PROFILE

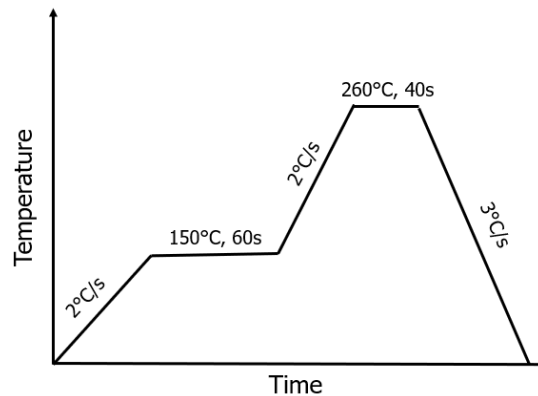


Figure 6: Solder Reflow Profile

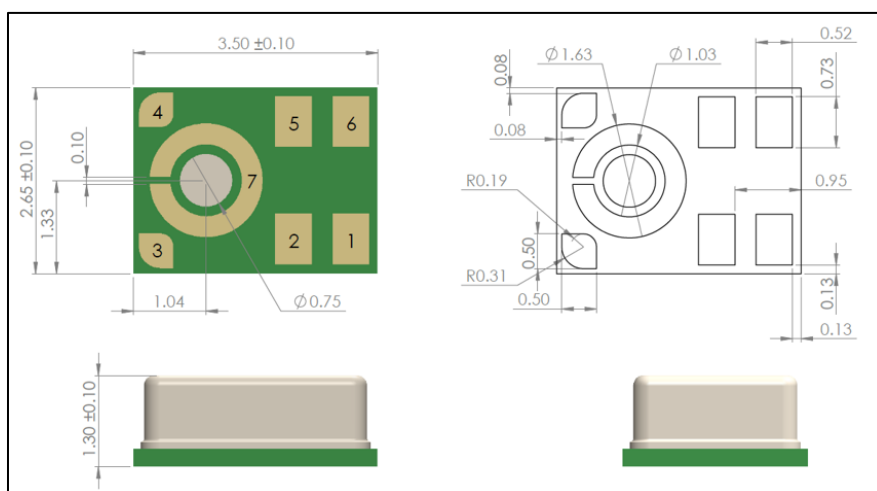
HANDLING INSTRUCTIONS

The Piezo MEMS microphone is very robust to harsh environments such as dust and moisture. However, to avoid mechanical damage to the mic we recommend using appropriate handling procedures when manually handling the parts or when using pick and place equipment. The following guidelines will avoid damage:

- Do not apply a vacuum to the bottom side of the microphone. A vacuum pen may be used with care on the top side only.
- Do not apply very high air pressure over the port hole.
- Do not insert any large particles or objects in the port hole. The microphone is robust to small particles per IP5x specification.
- Do not board wash or clean after the reflow process or expose the acoustic port to harsh chemicals.

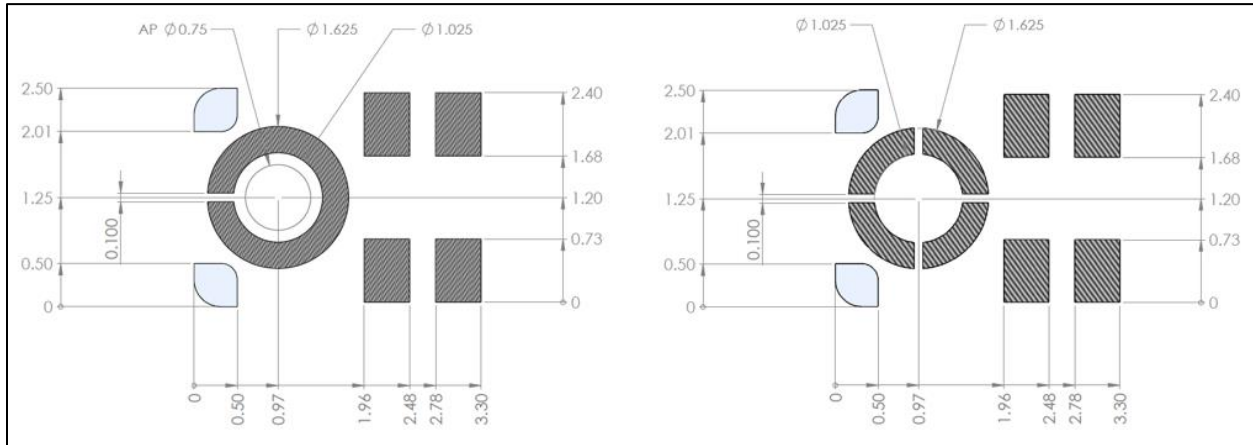
Please refer to this [Application Note](#) for Microphone Assembly Guidelines.

DIMENSIONS AND PIN LAYOUT



Pin Number	Pin Name	Description
1	DATA	PDM Digital Output
2	L/R SELECT	Left/Right Channel Select
3	NC	No Connect
4	NC	No Connect
5	CLK	Clock
6	VDD	Power Supply
7	GND	Ground

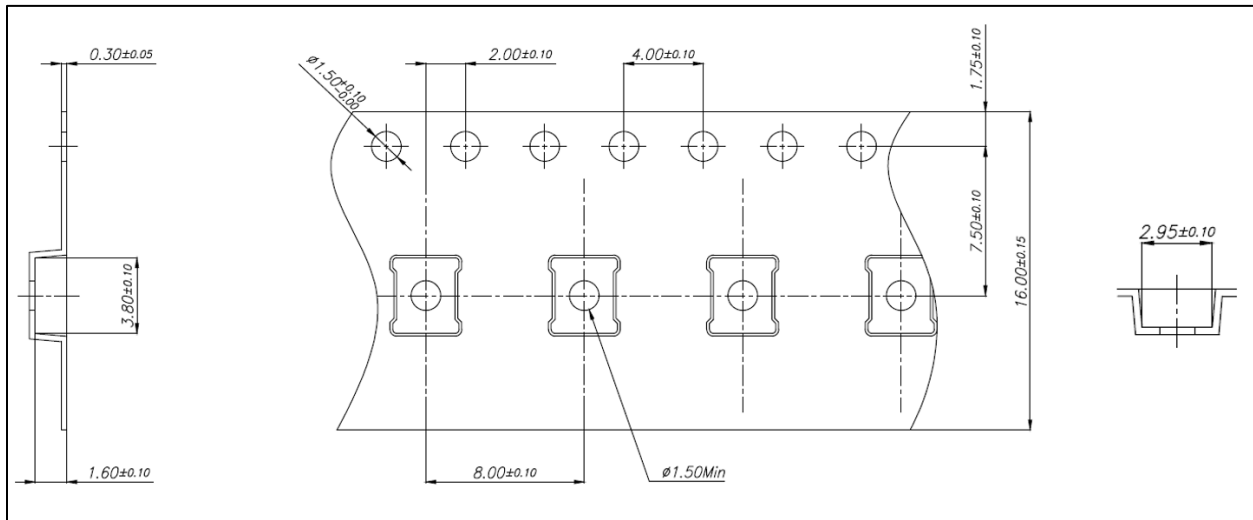
PCB DESIGN AND LAND PATTERN LAYOUT



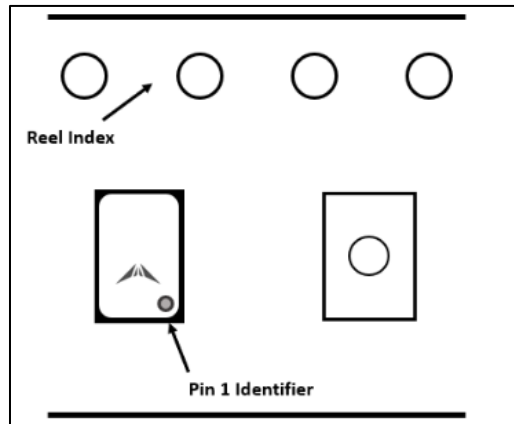
PCB and Solder Stencil Pattern – All dimensions are in mm

Lightly shaded pads are No Connect and are optional for the footprint. If they are included they should be left floating.

TAPE AND REEL SPECIFICATIONS

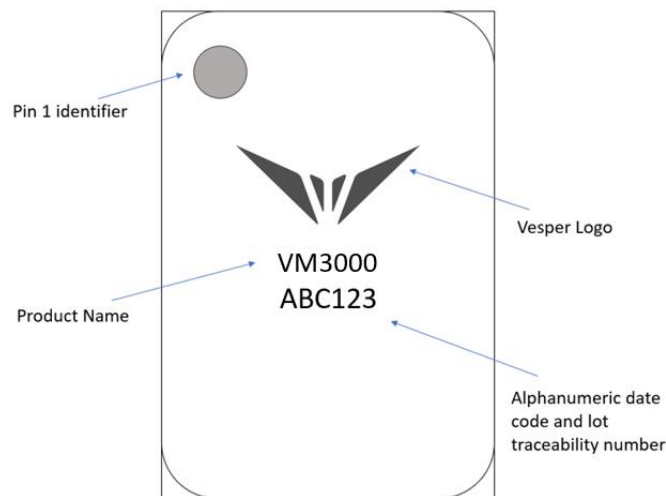


Tape and Reel specification - All dimensions in millimeters



Part Orientation in Reel (Note: Dimensions not to scale)

LID MARKING



Lid Marking Description

SUPPORTING DOCUMENTS

VM3000_Coupon_PCB_UserGuide - Vesper VM3000 Coupon PCB board user guide

VM3000_3D_Model – Vesper VM3000 3D CAD Layout

AN3 – Vesper Piezoelectric MEMS Microphone Assembly Guidelines

COMPLIANCE INFORMATION

Electrostatic discharge (ESD) sensitive device:

Although this product features industry standard protection circuitry, damage may occur if subjected to excessive ESD. Proper precautions should be taken to avoid damage to the device.

**CONTACT DETAILS**

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LEGAL INFORMATION

For any questions or comments on the datasheet email: erratum@vespermems.com

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REVISION HISTORY

Revision	Date	Description
0.0.0	02/22/2019	Initial Revision
0.0.1	07/16/2019	Updated Low Power Mode Numbers, Fixed Typo Updated 3dB roll off to 100Hz nominal
0.0.2	07/29/2019	Updated performance metrics
0.0.3	08/15/2019	Added Typical Performance Curves, SELECT Functionality, Updated Tape and Reel Drawings
0.0.4	09/12/2019	Updated Device Modes Power Consumption Table
0.0.5	09/17/2019	Updated PCB Land Pattern Drawing
0.0.6	10/21/2019	Updated IPx7 rating to IPx8 Updated ESD-HBM test limit from 2kV to 4kV
0.0.7	12/29/2019	Fixed typo in Timing Table
0.0.8	1/31/2020	Updated SNR, PSRR values Updated Frequency Response and THD curves